

## REMARKS

Claims 8-11 and 22-35 are now pending in the application. Claims 1-7 and 12-21 have been cancelled. Claims 26-35 have been added herein. Support for the subject matter in new Claims 26 and 30 can be found at least in paragraph [0124] wherein the example states that the silicon oxide layer is formed by reduced CVT method using TEOS. A formula of TEOS is  $C_8H_{20}O_4Si$ , which does not comprise boron and phosphorus. No new matter has been added. Claims 8-11 and 22-25 stand rejected. The Examiner is thanked for the telephonic interview of August 10, 2004. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

## DRAWINGS

The drawings stand objected to for certain informalities. Specifically, the Examiner states Figure 18 should be designated by a legend such as –Prior Art–. Applicants have attached revised drawings for the Examiner's approval. In the “Replacement Sheets” Figure 18 has been amended to include the legend “Prior Art.” It is believed that with this addition, the objection is now rendered moot. Accordingly, approval of the “Replacement Sheets” and withdrawal of the instant objection are requested.

## SPECIFICATION

The specification stands objected to for certain informalities. The Examiner states that the title of the invention is not descriptive and that a new title is required that is clearly indicative of the invention to which the claims are directed. The title has been

amended herein to read "SEMICONDUCTOR DEVICE HAVING A NON-VOLATILE MEMORY TRANSISTOR FORMED ON A SEMICONDUCTOR LAYER." It is believed that this new title is clearly indicative of the invention to which the claims are directed. Accordingly, reconsideration and withdrawal of the instant objection are requested.

**REJECTION UNDER 35 U.S.C. § 103**

Claims 8, 11, 22 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Goda et al. (U.S. Publication No. 2001/002713) in view of Machida et al. (U.S. Pat. No. 5,376,590). This rejection is respectfully traversed.

Claims 8 and 22 both call for the interlayer dielectric layer including/comprising "a first oxide film provided as a lowermost layer of the interlayer dielectric, a layer containing nitride provided on and in direct contact with the first oxide film." In the Office Action, it is stated that the Goda et al. reference fails to disclose this subject matter. The Office Action then relies upon the Machida et al. reference as teaching that a first oxide film would protect Goda's device against contamination by mobile ions. The motivation to provide a first oxide film as the lowermost layer of Goda's dielectric layer, as suggested by Machida et al., is to protect the device against contamination by mobile ions. It is respectfully submitted, however, that Goda does not disclose nor suggest a necessity or a desirability to protect the device against contamination by mobile ions. With the Goda reference being completely unconcerned with protection against contamination from mobile ions, it is respectfully submitted that the fact that Machida et al. teaches use of an oxide film to protect the device against contamination by mobile ions is irrelevant. Accordingly, it is respectfully submitted that one skilled in the art

would not make the combination as suggested by the Examiner because there is no necessity nor reason to provide or protect against contamination by mobile ions in the Goda device. Accordingly, for at least this reason, it is respectfully submitted that the subject matter of Claims 8 and 22 is non-obvious and patentable over the priority record. Claims 11 and 25 depend from Claims 8 and 22 and, therefore, for at least the same reason stated above in reference to Claims 8 and 22, are also non-obvious and patentable over the priority record. Accordingly, withdrawal of the instant rejection is requested.

Claims 9, 10, 23 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Goda/Machida in view of Wu (U.S. Pat. No. 6,008,517). This rejection is respectfully traversed.

Claims 9 and 23 both call for “wherein the first oxide film has a thickness of 10 – 80nm.” Both claims 10 and 24 call for “wherein the first oxide film has a thickness of 30 – 70nm.” In rejecting these claims, the Office Action relies upon the Wu reference as showing that these thicknesses are in common use in similar devices in the art and that Applicants have not established the criticality of these ranges.

It is respectfully submitted that one would not look to the Wu reference to arrive at the subject matter of these claims. Specifically, the Wu reference does not disclose nor teach an oxide layer having these ranges and used in a manner as called for in these claims. Rather, the Wu reference discloses forming silicone oxide layers of specific thicknesses for use in forming a flash member. Specifically, the Wu reference discloses the use of a thin silicone oxide layer for inhibiting the field oxide (FOX) growth on an active region of a semiconductor substrate 10 (See column 4, lines 14-20 of the

Wu reference), a first oxide layer 16 that serves as a tunneling oxide layer (See column 4, lines 48-65 of the Wu reference), and a second oxide layer 22 that serves as an insulation oxide over the junction region 20 (See column 5, lines 15-28 of the Wu reference). All these various oxide layers are used to form the internal components of the flash memory. None of these layers are used to form an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor. In other words, the Wu reference may teach specific film thicknesses for use in forming a non-volatile memory transistor, but it does not disclose any types of films or thicknesses for use as an interlayer dielectric layer that is provided over the non-volatile memory transistor. Accordingly, since the Wu reference is completely unconcerned with the interlayer dielectric layer, it is respectfully submitted that one skilled in the art would not look to the Wu reference for teachings associated with oxide film thicknesses to form an interlayer dielectric layer over a non-volatile memory transistor as called for in the claims. Thus, it is respectfully submitted that the Wu reference does not provide any teachings, suggestions nor motivation to one skilled in the art to form an interlayer dielectric layer having the specific thicknesses and over a non-volatile memory transistor as called for in claims 9, 10, 23 and 24. Accordingly, for at least these reasons it is respectfully submitted that claims 9, 10, 23 and 24 are non-obvious and patentable over the prior art of record and withdrawal of the instant rejection is requested.

Furthermore, it is respectfully submitted that the thicknesses of the oxide film called for in at least claims 10 and 24 are critical to the invention as clearly stated in the specification and shown in Figure 17. Specifically, the thickness of 30 – 70nm has been

discovered to produce unexpected and advantageous results. Referring to Experimental Example 2 in the present application (See paragraphs [0123] to [0127], [0016] and [0085] and Figure 17 of the present application) the inventors have discovered that by forming the oxide film with these specific dimensions unexpectedly provides an oxide film that: (1) inhibits the amount of change in the threshold voltage on the control gate; and (2) stabilizes the memory characteristics while the rewritable number required for a memory can be maintained. Specifically, as stated in paragraph [0126] and shown in Figure 17, the inventors have discovered that Delta WL-Vth values sharply drop when the silicone oxide film becomes 30nm or greater. Thus, in order to inhibit the amount of change in threshold voltage on the control gate and stabilize the memory characteristic, it is critical to have a silicone oxide film of 30nm or greater. Further, as stated in paragraph [0126] and shown in Figure 17, the inventors have also discovered that maintaining FTUR (a rate of potential change that appears in a specified reference current flown for a predetermined period of time) to a value of 1.2 or lower is achieved when the film thickness is 70nm or less. When the value of FTUR is maintained to 1.2 or lower, the rewritable number required for a memory can be maintained. This means that when the film thickness is 70nm or less, the required rewritable number can be maintained. Thus, it is critical to maintain the film thickness to 70nm or less. Accordingly, it is critical to the invention to maintain the silicone oxide film between 30nm and 70nm to achieve the unexpected results that the characteristics required in view of the rewritable number can be maintained and the memory characteristic can be stabilized while inhibiting amounts of change in the threshold voltage on the control gate. Thus, it is respectfully submitted the specification and

drawings establish the criticality of the numerical range called for in at least claims 10 and 24. Accordingly, for at least this additional reason it is respectfully submitted that the subject matter of claims 10 and 24 is non-obvious and patentable over the prior art of record and withdrawal of the instant rejection is requested.

### **New Claims**

Claims 26 and 30 both call for “wherein . . . the first oxide film is free of boron and phosphorus.” It is respectfully submitted that this subject matter is not disclosed nor suggested in the prior art of record. The Goda et al. reference fails to disclose the first oxide film as called for in the claims. Furthermore, the oxide film of the Machida et al. reference teaches that the film requires the use of an oxide of boron or phosphorus. (See at least column 15, lines 9-19 and column 15, line 55 – column 16, line 7 of the Machida et al. reference.) The use of an oxide film containing an oxide of at least one of boron and phosphorus is in direct contrast to the first oxide film called for in claims 26 and 30 wherein the first oxide film is free of boron and phosphorus. Accordingly, for at least this reason it is respectfully submitted that the subject matter of new claims 26 and 30 is not disclosed, taught nor suggested in the prior art of record.

Claims 27-29 and 31-33 all depend from one of claims 26 and 30 and, therefore, for at least the same reason stated above with reference to claims 26 and 30, are also non-obvious and patentable over the prior art of record. Accordingly, allowance of Claims 26-33 is requested.

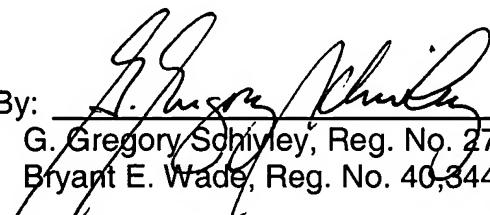
Referring now to new Claim 34, the claim calls for “the first oxide film is a thickness of 30-70nm.” For at least the reasons stated above, with reference to Claims

10 and 24, it is respectfully submitted that the subject matter of Claim 34 is non-obvious and patentable over the priority of record. New Claim 35 depends from Claim 34 and, therefore, for at least the same reasons stated above with reference to Claim 34, is also non-obvious and patentable over the priority record. Accordingly, allowance of new Claims 34 and 35 is requested.

**CONCLUSION**

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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